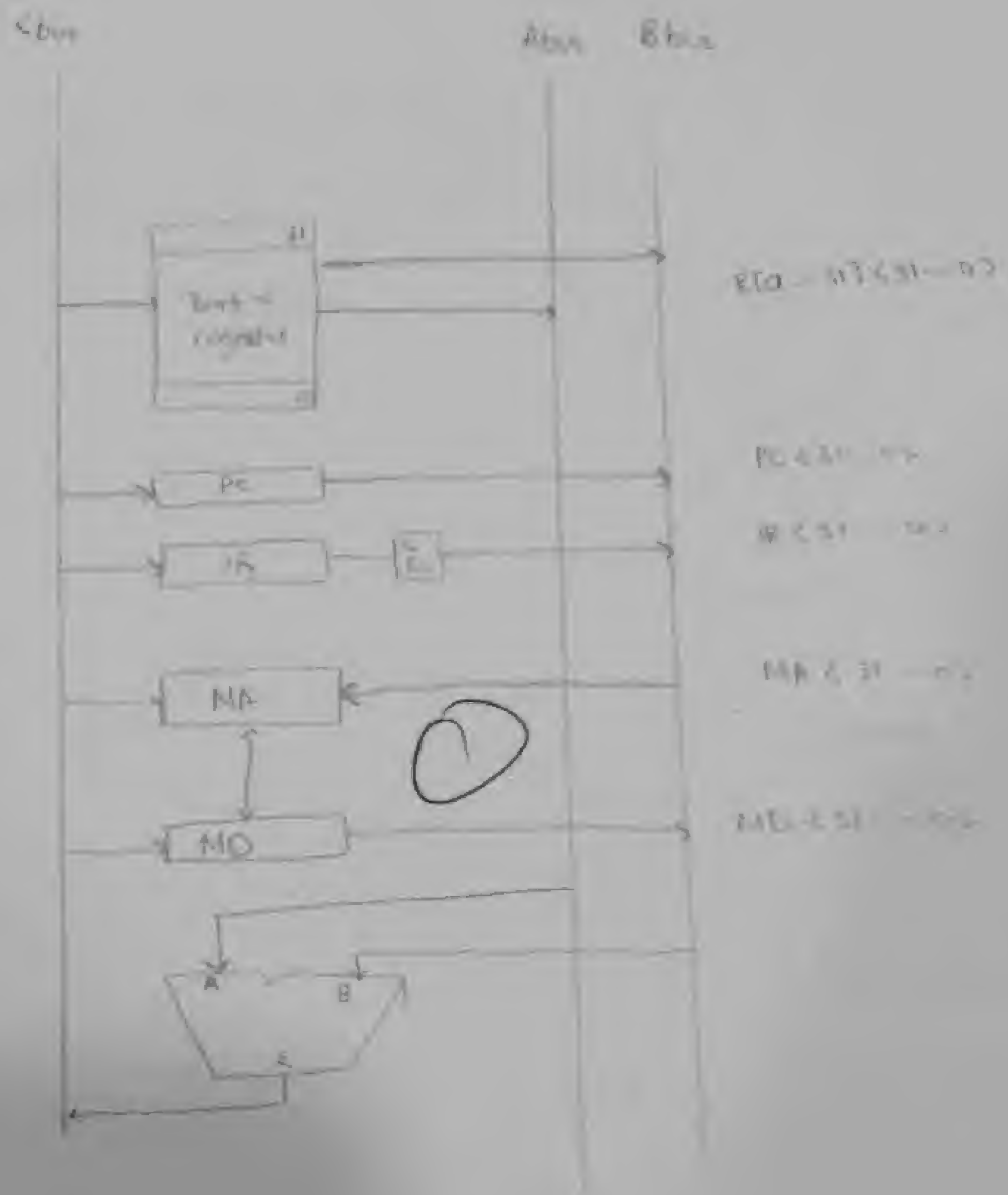


Q1:

A) Draw a complete high level architecture of a 3- Bus SRC processor. (6 marks)



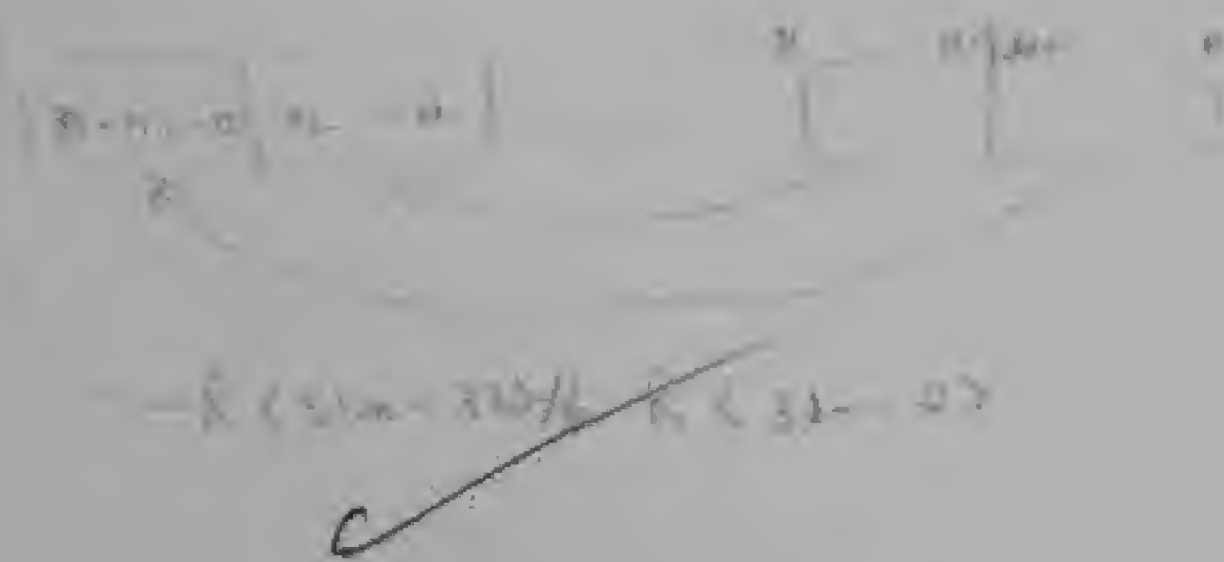
B) Write the concrete RTN of the following instructions assuming 3- Bus system:

i. shc

(4 marks)

$T_0 - T_1$ Fetch
 T_2 $r \leftarrow R[4-0]$
 T_3 $(r \neq 0) (r \leftarrow R[r] \ll 4-0)$
 T_4 $SH(1) (r \ll 1) \leftarrow 0$
 T_5 $R[32] \leftarrow R[32] \ll 1$
 T_6 $R[32] \leftarrow R[32] \ll 1$

Control
Same
as
Page 4



2

ii. st

(4 marks)

$T_0 - T_1$ Fetch
 T_2 $MD \leftarrow R[4]$
 T_3 $MD \leftarrow (R[4] \ll 4) \oplus (R[4] \ll 8) \oplus (R[4] \ll 12) \oplus (R[4] \ll 16)$
 T_4 $MD \leftarrow MD \oplus R[4]$

MD ← R[4] + MD
 MD ← MD + MD
 MD ← MD + MD
 MD ← MD + MD

12

Fetch instruction
 T_0 $MA \leftarrow PC : PC \leftarrow PC + 4 ; MD \leftarrow MEM[MA]$
 T_1 $R \leftarrow MD$

PC ← PC + 4
 MD ← MD
 MD ← MD

C) Assuming that you are using 2-Bus System:

- i. Write the concrete RTN of she instruction using the 2-Bus system assuming that the value of n is $(00101)_2$ (4 marks)

Pr. 5

T 1000-100

$$T_1 \quad M_0 \leftarrow \text{MEIART} + PC \leftarrow PC + 4$$
$$T_{\text{eff}} = 1/R = 1000$$
$$T_3 \quad n \rightarrow \infty \quad 1R \subset n \rightarrow \infty$$

7. Ring 4 - Ring 6

$$1 \leq n \leq n_0 + 1, \exists k \in \mathbb{N}$$

Plum: $E = E_0 \sin \omega t$

$$Mg_{0.2} + P_{0.0001} + C_{0.0001} + H_{0.0001} + N_{0.0001} + O_{0.0001}$$
 $\mathbb{E}_{\text{data}} \approx 13$

Geo. Frost, Md.

Gr. Red, Sh. D. 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 8

ii. Given the following delays :

(8 marks)

Delay name	Value of the delay
Gate (Buffer) delay time	5 ns
Bus delay time	5 ns
Logic delay time	14 ns
Flip-Flop (Latch) delay	3 ns

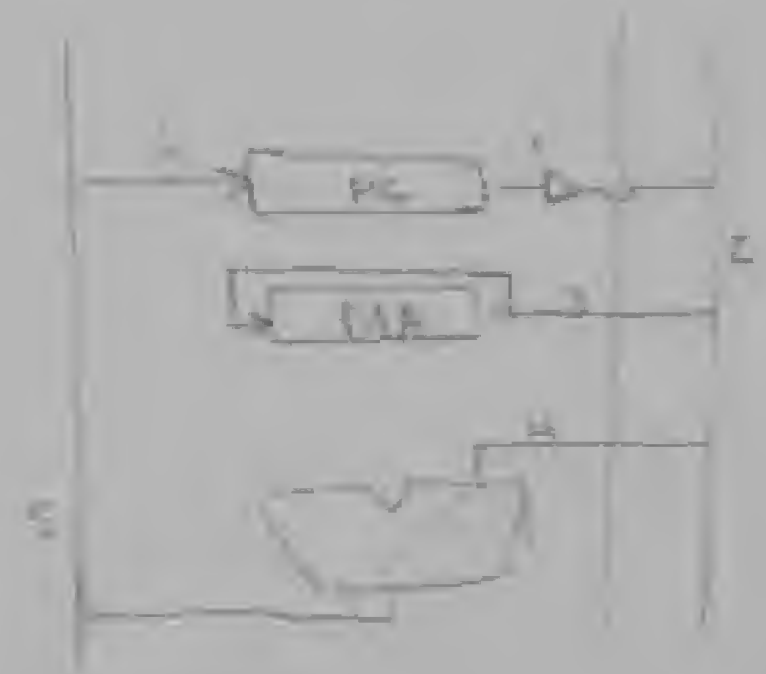
Assuming that the worst case delay can be estimated as the maximum delay of the instructions in step T_0 . Calculate the frequency of both 2-Bus and 3-Bus systems?

2-Bus

3-Bus

$T_0 \quad MA \leftarrow PC$

$T_0 \quad MA \leftarrow PC : PC \leftarrow PC + 4 : MD \leftarrow [MEMA]$



Buffer \rightarrow Bus \rightarrow ALU \rightarrow Bus \rightarrow latch

Buffer \rightarrow Bus \rightarrow latch \rightarrow ALU \rightarrow Bus \rightarrow latch

$$T = d_{buf} + d_{bus} + d_{alu} + d_{bus} + d_{latch}$$

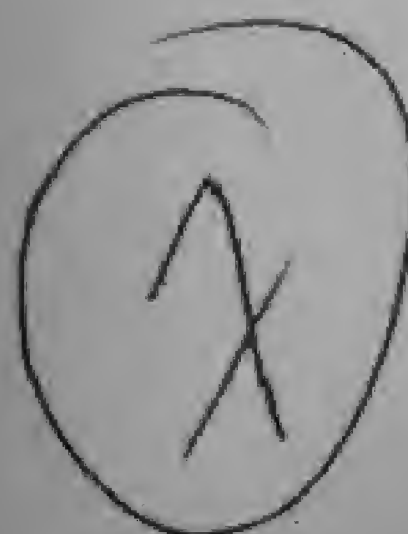
$$T = d_{buf} + d_{bus} + d_{latch} + d_{alu} + d_{bus} + d_{latch}$$

$$= 5 + 5 + 14 + 5 + 3 = 32$$

$$= 5 + 5 + 5 + 14 + 5 + 3 = 37$$

$$F = \frac{1}{T} = \frac{1}{32} = 0.03125 \text{ ns}$$

$$F_{req} = \frac{1}{T} = \frac{1}{37} = 0.027027 \text{ ns}$$



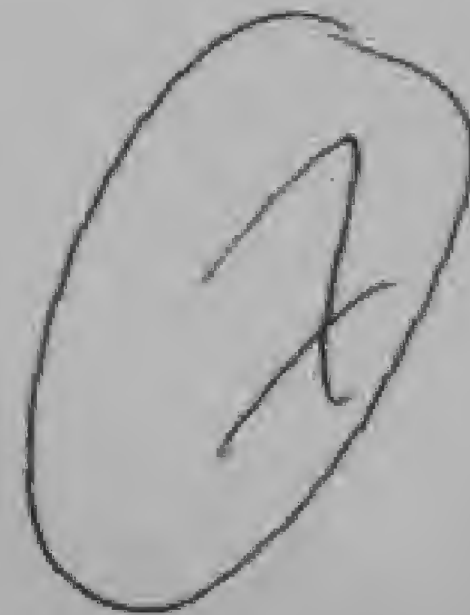
- iii. Using the information given in part A. i, and part B. i, and part B. ii, calculate the numerical speed up percentage if you are executing the instruction shc on a 3-Bus system over the case of executing the same instruction using a 2-Bus system? (8 marks)

$$\begin{aligned}
 & \text{2-bus} \\
 ET &= IC + \underline{CPI} \times T \\
 &= 1 + 11 \times \frac{1}{10} \\
 &= 352
 \end{aligned}$$

$$\begin{aligned}
 & \text{3-bus} \\
 ET &= IC + CPI \times T \\
 &= 1 + 10 \times \frac{1}{10} \\
 &= 350
 \end{aligned}$$

$$\begin{aligned}
 \text{Speed Up} &= \frac{\text{Time}_{\text{min}}}{\text{Time}_{\text{max}}} \times 100 \\
 &= \frac{352 - 350}{350} \times 100 \\
 &= 0.57\%
 \end{aligned}$$

+11-1



* Assume IC (Instruction Counter) = 1

* Assume min 3bus = (00101)
= 5

iv. Assume that there is extra three clock cycles are required in case of using a 2-Bus system to read from the memory, recalculate part iii using this assumption? (8 marks)

$$\text{CPI in 2bus} = 11 + 3 \text{ more} = 14$$

2-bus

$$\begin{aligned} ET &= IC \times CPI \times T \\ &= 1 \times 14 \times 32 \\ &= 448 \end{aligned}$$

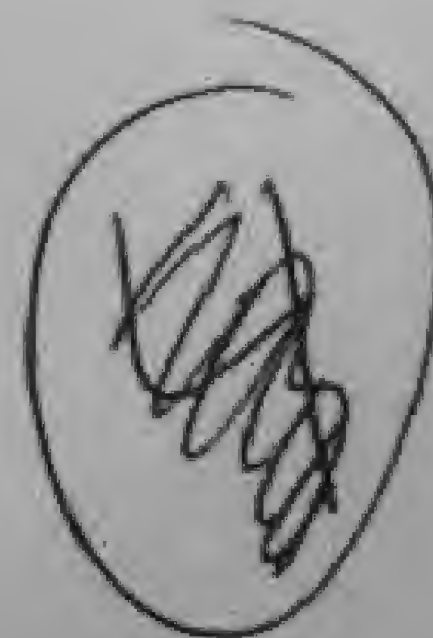
X

3bus

$$\begin{aligned} ET &= IC \times CPI \times T \\ &= 1 \times 10 \times 35 \\ &= 350 \end{aligned}$$

$$\text{Speed UP} = \frac{\text{max} - \text{min}}{\text{min}} \times 100$$

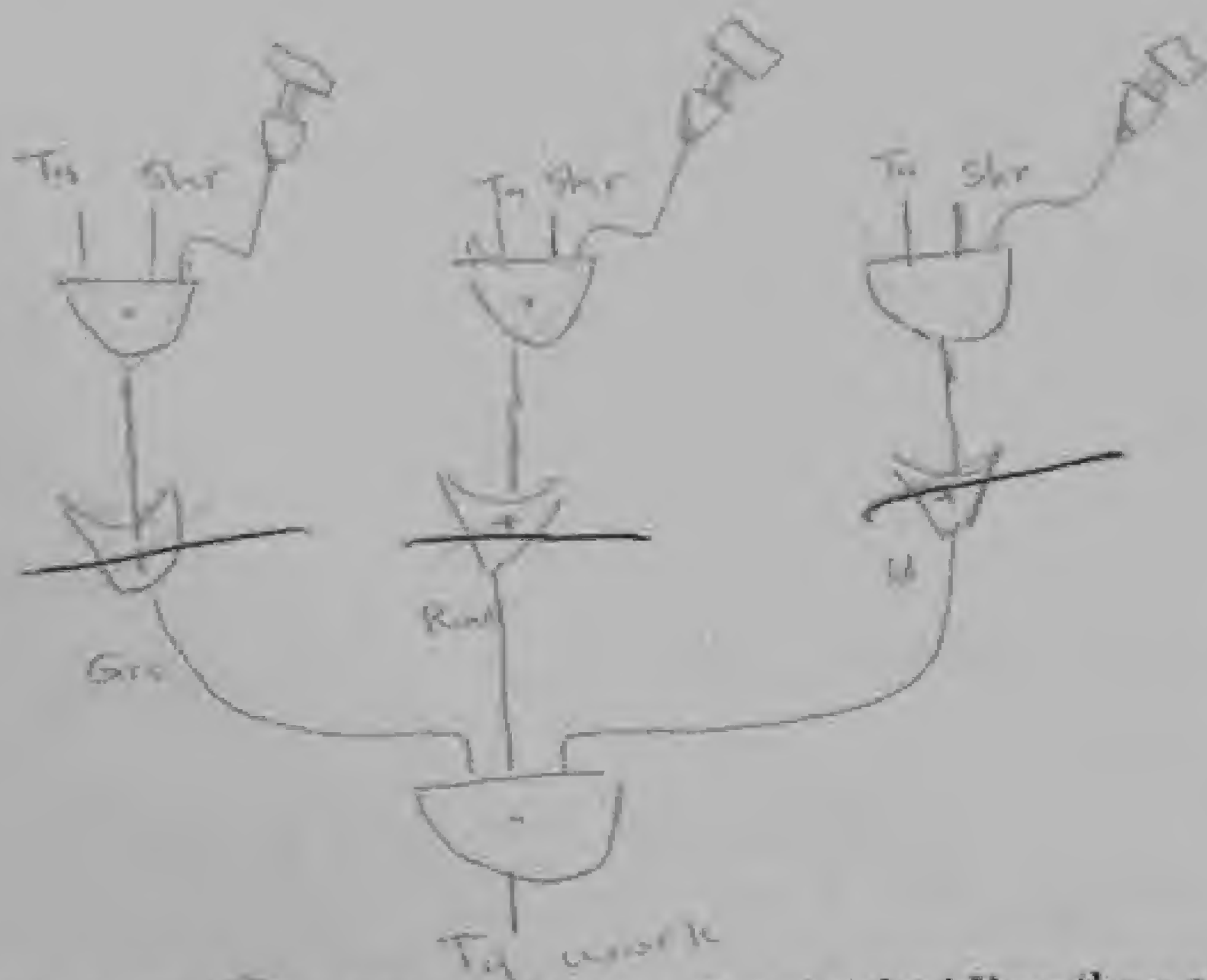
$$= \frac{448 - 350}{350} \times 100 = 28\%$$



Q2: Answer the following questions:

- i. Implement the control signals Grc, Rout, and Ld in the following step of shr operation using 1-Bus system. Assume all required logic gates. (8 marks)

	Instruction	Control Signals
T ₄	$n \neq 0 \rightarrow (n \leftarrow R[rc] \ll 4 \dots 0);$	$n \neq 0 \rightarrow (Grc, Rout, Ld)$



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- ii. The instruction $PC \leftarrow PC + N$, what are the two factors deciding the value of N? (4 marks)

- Size of mem \rightarrow
- Size of IR



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iii. Assume that we do not have the bank of register in the 1-Bus system. Discuss if this may be cause any problem or not? (6 marks)

bank of register is Cache memory

- the speed of CPU is very very high and the speed of memory is slow if CPU match speed of memory (don't use the bank of register) this will slow down the processor

So we use the cache to solve this problem we should use hierarchy (step by step) to communicate



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